In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Canceled)

2. (Currently Amended) A time division multiplex data recover system comprising:

a reference clock generator generating a reference clock signal;

a phase frequency comparator having a first input connected to said reference clock generator, a second input and an output generating a voltage proportional to a difference in phase and frequency between a signal received at said first input and a signal received at said second input;

a voltage controlled oscillator having a voltage input connected to said output of said phase frequency comparator and plural outputs each generating a corresponding ~~signals~~ clock signal at differing phases, each having a frequency proportional to a voltage received at said voltage input, said plural clock signals including a sampling clock signal and a leading clock signal having a phase leading said sampling clock signal by 90°;

a data recovery block having an input receiving a time division multiplexed data signal ~~and plural clock inputs, each clock input connected to a corresponding one of said plural outputs of said voltage controlled oscillator~~, a first clock input receiving said sampling clock signal and a second clock input receiving said leading clock signal, said data recovery block deserializing the received time division multiplexed data signal by sampling with said sampling clock signal, said data recovery block further sampling the received time division multiplexed data signal with said leading clock and generating an early/late signal

indicating whether said sampling clock signal is early or late by comparing the received time division multiplexed data signal sampled with said sampling clock signal to the received time division multiplexed data signal with said leading clock;

a phase selection circuit connected to said data recovery block ~~selecting two of said clock outputs of said voltage controlled oscillator adjacent in phase~~ and receiving said early/late signal, said phase selection circuit generating an interpolation code indicative of an interpolation amount and a phase select code indicative of one of said plural clock signal of said voltage controlled oscillator dependent upon ~~said data recovery error signals~~ said early/late signal;

a phase ~~interpreter~~ interpolator having ~~first and second~~ plural clock inputs receiving said ~~two clock outputs of said phase selection circuit~~ plural clock signals at differing phases of said voltage controlled oscillator, an interpolation input receiving said interpolation code and a phase select input receiving said phase select code, and phase interpolator generating a single output signal of an interpolation of ~~said first and second inputs~~ two clock signals of adjacent phases corresponding to said ~~data recovery signals~~ interpolation code and said phase select code, said single output signal connected to said second input of said phase frequency comparator.

3. (Preciously Added) The time division multiplex data recover system of claim 2, wherein:

said voltage controlled oscillator includes a ring oscillator having a plurality of differential input, differential output voltage controlled delay elements, said differential outputs of said voltage controlled delay elements forming said plural outputs of said voltage controlled oscillator.